WHAT IS CLAIMED IS:

1. A semiconductor integrated circuit comprising:

a logic circuit section formed of a plurality of first transistors of a first conductivity type and a plurality of second transistors of a second conductivity type, the logic circuit section being controlled according to an input signal;

a third transistor of the first conductivity type configured to supply power to the logic circuit section;

a fourth transistor of the second conductivity type connected to an output terminal of the logic circuit section, the fourth transistor setting a level at the output terminal when the logic circuit section does not operate;

a first control signal used to control the first and second transistors; and

a second control signal different from the first control signal and used to control the third transistor.

2. The circuit according to claim 1, wherein threshold voltages of the first to fourth transistors are set to have a single absolute value.

3. The circuit according to claim 1, wherein a high level of the first control signal is a first voltage, and a low level of the first control signal is a second voltage lower than the first voltage, a high

level of the second control signal being the first voltage, a low level of the second control signal being a third voltage lower than the second voltage.

4. The circuit according to claim 3, wherein the third voltage is a negative voltage.

5. The circuit according to claim 1, wherein an absolute value of threshold voltages of the first and second transistors of the logic circuit section is set to a first threshold voltage, the third transistor being set to have a second threshold voltage whose absolute value is higher than an absolute value of the first threshold voltage, the fourth transistor being set to have one of the first and second threshold voltages.

6. The circuit according to claim 5, wherein the third and fourth transistors are controlled by a single voltage.

7. A semiconductor integrated circuit comprising:

a logic circuit section formed of a plurality of first transistors of a first conductivity type and a plurality of second transistors of a second conductivity type, the logic circuit section being controlled according to an input signal;

a third transistor of the second conductivity type configured to supply power to the logic circuit section;

a fourth transistor of the first conductivity type

connected to an output terminal of the logic circuit section, the fourth transistor setting a level at the output terminal when the logic circuit section does not operate;

a first control signal used to control the first and second transistors;

a second control signal used to control the third transistor; and

a third control signal used to control the fourth transistor.

8. The circuit according to claim 7, wherein threshold voltages of the first to fourth transistors are set to have a single absolute value.

9. The circuit according to claim 7, wherein a high level of the first control signal is a first voltage, and a low level of the first control signal is a second voltage lower than the first voltage, a high level of the third control signal being the first voltage, a low level of the third control signal being a third voltage lower than the second voltage.

10. The circuit according to claim 9, wherein the third voltage is a negative voltage.

11. The circuit according to claim 9, wherein a high level of the second control signal is a fourth voltage higher than the first voltage.

12. The circuit according to claim 7, wherein an absolute value of threshold voltages of the first

and second transistors of the logic circuit section is set to a first threshold voltage, the third transistor being set to have a second threshold voltage whose absolute value is higher than an absolute value of the first threshold voltage, the fourth transistor being set to have one of the first and second threshold voltages.

13. The circuit according to claim 7, wherein the third and fourth transistors are controlled by a single voltage.

14. A semiconductor integrated circuit comprising:

a first node supplied with a first power supply voltage;

a second node supplied with a second power supply voltage lower than the first power supply voltage;

a logic circuit section formed of a plurality of first transistors of a first conductivity type and a plurality of second transistors of a second conductivity type, the logic circuit section being controlled according to an input signal, a current path of each of the second transistors having one end connected to the first node, and another end connected to an output terminal of the logic circuit section;

a third transistor of the first conductivity type connected between the logic circuit section and the second node;

a fourth transistor of the second conductivity

type connected between the first node and the output terminal of the logic circuit section, the fourth transistor setting a level at the output terminal to the first power supply voltage when the logic circuit section does not operate;

a first control signal used to control the first and second transistors;

a second control signal different from the first control signal and used to control the third transistor; and

a third control signal different from the first control signal and used to control the fourth transistor.

15. The circuit according to claim 14, wherein threshold voltages of the first to fourth transistors are set to have a single absolute value.

16. The circuit according to claim 14, wherein a high level of the first control signal is a first voltage, and a low level of the first control signal is a second voltage lower than the first voltage, a high level of the second control signal being the first voltage, a low level of the second control signal being a third voltage lower than the second voltage, a high level of the third control signal being a fourth voltage higher than the first voltage.

17. The circuit according to claim 16, wherein the third voltage is a negative voltage.

18. The circuit according to claim 14, wherein an absolute value of threshold voltages of the first and second transistors of the logic circuit section is set to a first threshold voltage, the third transistor being set to have a second threshold voltage whose absolute value is higher than an absolute value of the first threshold voltage, the fourth transistor being set to have one of the first and second threshold voltages.

19. The circuit according to claim 18, wherein the third and fourth transistors are controlled by a single voltage.

20. A semiconductor integrated circuit comprising:

a first node supplied with a first power supply voltage;

a second node supplied with a second power supply voltage lower than the first power supply voltage;

a logic circuit section formed of a plurality of first transistors of a first conductivity type and a plurality of second transistors of a second conductivity type, the logic circuit section being controlled according to an input signal, a current path of each of the first transistors having one end connected to an output terminal of the logic circuit section, and another end connected to the second node;

a third transistor of the second conductivity type connected between the logic circuit section and the

first node;

a fourth transistor of the first conductivity type connected between the output terminal of the logic circuit section and the second node, the fourth transistor setting a level at the output terminal to the first power supply voltage when the logic circuit section does not operate;

a first control signal used to control the first and second transistors;

a second control signal different from the first control signal and used to control the third transistor; and

a third control signal different from the first control signal and used to control the fourth transistor.

21. The circuit according to claim 20, wherein threshold voltages of the first to fourth transistors are set to have a single absolute value.

22. The circuit according to claim 20, wherein a high level of the first control signal is a first voltage, and a low level of the first control signal is a second voltage lower than the first voltage, a high level of the second control signal being a third voltage higher than the first voltage, a low level of the second control signal being the first voltage, a high level of the third control signal being a fourth voltage higher than the first voltage, a low level of

the third control signal being a fifth voltage lower than the second voltage.

23. The circuit according to claim 22, wherein the fifth voltage is a negative voltage.

24. The circuit according to claim 22, wherein an absolute value of threshold voltages of the first and second transistors of the logic circuit section is set to a first threshold voltage, the third transistor being set to have a second threshold voltage whose absolute value is higher than an absolute value of the first threshold voltage, the fourth transistor being set to have one of the first and second threshold voltages.

25. The circuit according to claim 24, wherein the third and fourth transistors are controlled by a single voltage.